ADM-VA601
User Manual

Document Revision: 1.0
3rd Feb 2025

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1 Introduction

The **ADM-VA601** is the base board at the core of the ADK-VA601 Versal Development Platform for Space 2.0.

1.1 Key Features

Key Features

- VPX 6U Form Factor
- Supports the Versal Core VC1902 (LEO) Grade ACAP device in the 2197 pin package
- 2x Banks of space grade DDR4 SDRAM (with ECC)
- FMC+ front panel interface:
  - 24 high speed serial channels capable of 32Gbps each
  - 160 single ended general purpose signals (80 differential pairs)
  - 1.5-1.0V VADJ voltage range
- Voltage, current and temperature monitoring
- VPX P1 to P4 utilized according to OpenVPX payload slot profile SLT6-PAY-4F1Q2T-10.2.1
- Versatile MIO interface support:
  - Ethernet
  - GPIO
  - uSD
  - Dual QSPI
  - UART
- Voltage and temperature monitoring
- User LEDs and switches
- Air-cooled and conduction-cooled configurations

1.2 References & Specifications

ANSI/VITA 46.0	*VPX Baseline Standard*, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.4	*PCI Express® on the VPX Fabric Connector*, July 2010, VITA, Draft 0.15
ANSI/VITA 46.6	*Gigabit Ethernet Control Plane on VPX*, September 2010, VITA, Draft 0.7
ANSI/VITA 46.11	*System Management on VPX*, June 2015, VITA, ISBN 1-885731-84-1
ANSI/VITA 48.2	*Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX*, July 2010, VITA, ISBN 1-885731-60-4
ANSI/VITA 57.1	*ACAP Mezzanine Card (FMC) Standard*, July 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 65	*OpenVPX™ System Specification*, June 2010, VITA, ISBN 1-885731-58-2
ANSI/VITA 57.4	*ACAP Mezzanine Card Plus(FMC+) Standard*, March 2016, VITA, Draft
ANSI/VITA 78	*Space VPX System*, Feb 2015, VITA, ISBN 1-885731-83-3

Table 1 : References

1.3 Order Code

ADM-VA601(T)

Name	Symbol	Configurations
Configuration	T	/DEV - ADM-VA601/DEV - with XCVC1902 fitted purchasable as part of ADK-VA601 Development Kit /CC4 - build to order with Space Qualified Components /C(x) - build to order with Customer Specific Modifications

Table 2 : Build Options

Not all combinations may be available. Please check with Alpha Data sales for details.

2 Installation

2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VA601 is a 6U Space VPX reference platform for the AMD Versal AI Core XQRVC1902 Adaptable SoC platform for Space 2.0.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P1 to P4 IO and control lanes (Part number: ADM-VA600-RTM).

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the ACAP application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with AMD power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and appropriate metalwork for conduction cooled applications.

The board features system monitoring that measures the board and ACAP temperature. It also includes a self-protection mechanism that will clear the ACAP configuration if an over-temperature condition is detected.

See Section System Monitoring for health monitoring details.

Figure 1 : ADM-VA601

2.3 Software Installation

Please refer to the Reference Designs on the Alpha Data Download Site. Example projects for configuring the Versal ACAP device and example software for running on the ARM CPUs can be downloaded from there.

2.4 Order Code

See the ADM-VA601 web page for complete ordering options.

3 Board Information

3.1 Physical Specifications

The ADM-VA601 complies with vita 78 (6U / 220mm space VPX).

Description	Measure
Total Dy	233.34 mm
Total Dx	229.61 mm
PCB Dx	220 mm
Total Dz	20.32 mm
Circuit assembly weight	?? grams
Total weight (with heat sink)	?? grams

Table 3 : Mechanical Dimensions

3.2 Chassis Requirements

3.2.1 Mechanical Requirements

A 6U VPX rack is required for mechanical compatibility.

3.2.2 Power Requirements

The ADM-VA601 is powered via the +12V VPX power rail, all the internal power rails are generated from this rail.

The ADM-VA601 is capable of drawing up to 20A on the +12V VPX power rail.

The ADM-VA601 also requires the presence of a +3.3V_AUX auxiliary power rail, used to power monitoring and reset circuitry.

The ADM-VA601 is capable of drawing up to 100mA on the +3.3V_AUX power rail, this rail is supplied externally by default but can be generated internally via a build option.

Power consumption estimation requires the use of the AMD XPE spreadsheet (www.xilinx.com/products/technology/power/xpe.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85-0.90	VCC_INT	150A
0.85-0.90	VCC_IO + VCC_PSFP + VCC_RAM + VCC_SOC	10A
0.85-0.90	VCC_PSLP + VCC_PMC	2A
0.88	MGTAVCC	7A
1.2	MGTAVTT	8A
1.2	VCCO + DDR4	10A
1.5	VCCO + VCCAUX + VCCAUX_PMC	9A
1.0-1.5	FMC_VADJ + VCCO	6A
3.3	VCCO + FMC+	6A

Table 4 : Available Power By Rail

3.3 Thermal Performance

If the ACAP core temperature exceeds 105 degrees Celsius, the ACAP design will be cleared to prevent the card from over-heating.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the AMD Power Estimator (XPE) downloadable at www.xilinx.com/products/technology/power/xpe.html. Download the Versal tool and set the device according to your part number details: Versal AI Core Series, XCVC1902, VSVA2197 package, -2MS/-3HS speed grade, extended. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA. Then enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the VA601 power estimator from Alpha Data by contacting **support@alpha-data.com**. Enter in the power figures from XPE, FMC+ (if used), and DRAM utilization into the Alpha Data spreadsheet to get a complete board level estimate.

3.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products.

Please contact **sales@alpha-data.com** to obtain a quote and start your project today.

4 Functional Description

4.1 Overview

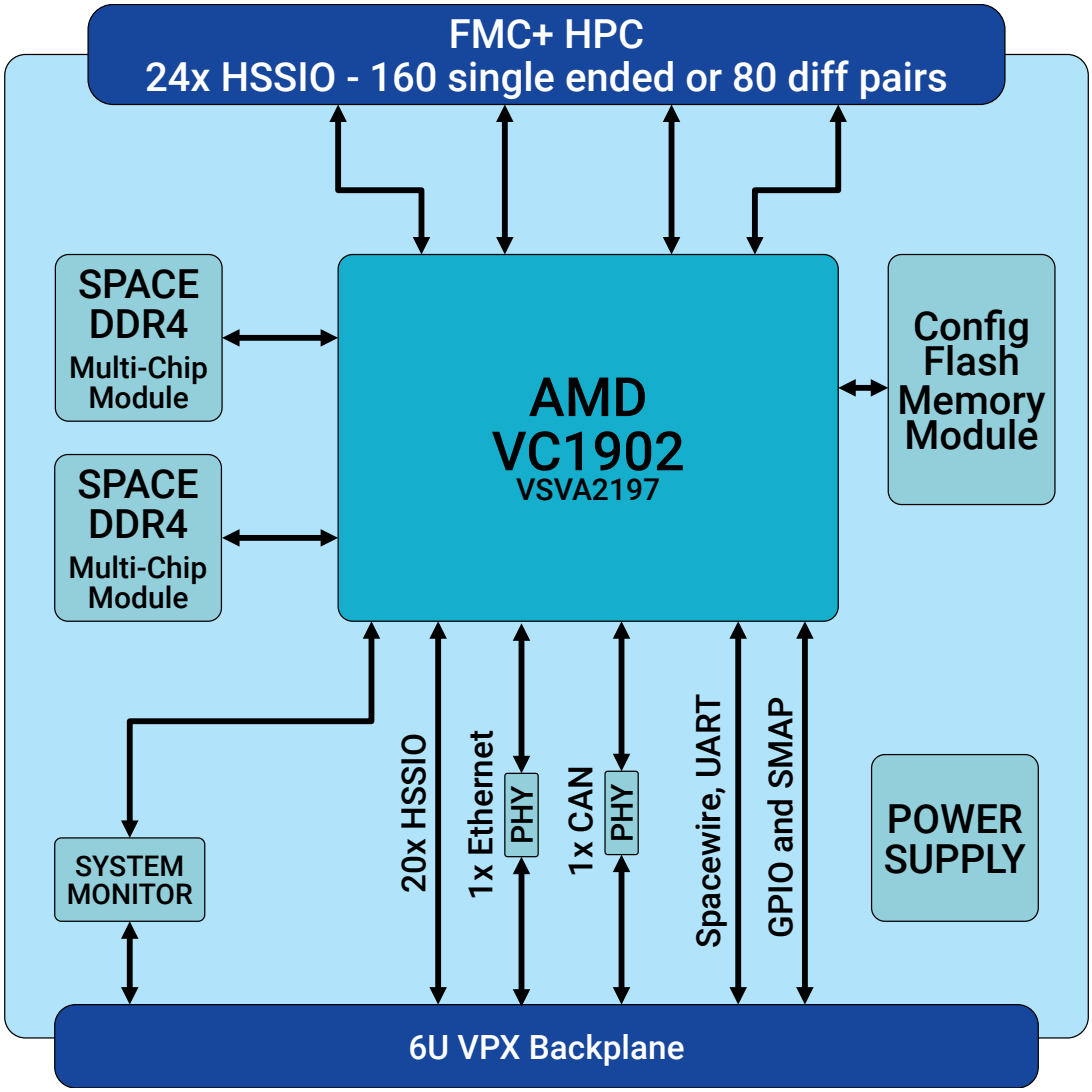

Figure 2 : ADM-VA601 Block Diagram

4.1.1 Switch Definitions

There are two sets of eight DIP switches placed on the bottom of the board. Their functions are described below.

> **Note:**
> All switches are OFF by default. Factory Configuration switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	User Switch 1	Pin AT6=logic low	Pin AT6=logic high
SW1-2	User Switch 2	Pin AR6=logic low	Pin AR6=logic high
SW1-3	User Switch 3	Pin AN6=logic low	Pin AN6=logic high
SW1-4	User Switch 4	Pin AN5=logic low	Pin AN5=logic high
SW1-5	VPX JTAG	Connect JTAG chain to P0	Isolate JTAG chain from P0
SW1-6	Factory Test	-	Normal Operation
SW1-7	Factory Configuration	-	Normal Operation
SW1-8	LPMODE_EN	Low power mode enabled	Normal Operation

Table 5 : VPX Control Switch Definitions (SW1)

Switch Ref.	Function	ON State	Off State
SW2-(4:1)	PS_MODE(3:0)	PS Boot Mode - see section Boot Modes	
SW2-5	Hardware Reset	Hardware Reset (complete restart)	Normal Operation
SW2-6	FMC_VADJ_E-EPROM	Use on board eeprom to configure FMC_VADJ supply	Normal Operation
SW2-7	SDCard_SEL	SMAP boot mode	SCard boot mode
SW2-8	VPX_IO_EN	VPX MIO IO Enabled	VPX MIO IO disabled

Table 6 : Processor Setup Switch Definitions (SW2)

4.1.2 LED Definitions

There are seven LEDs on the rear of the board which can be used to provide a visual indication of the board status.

Their locations are shown in Figure 3

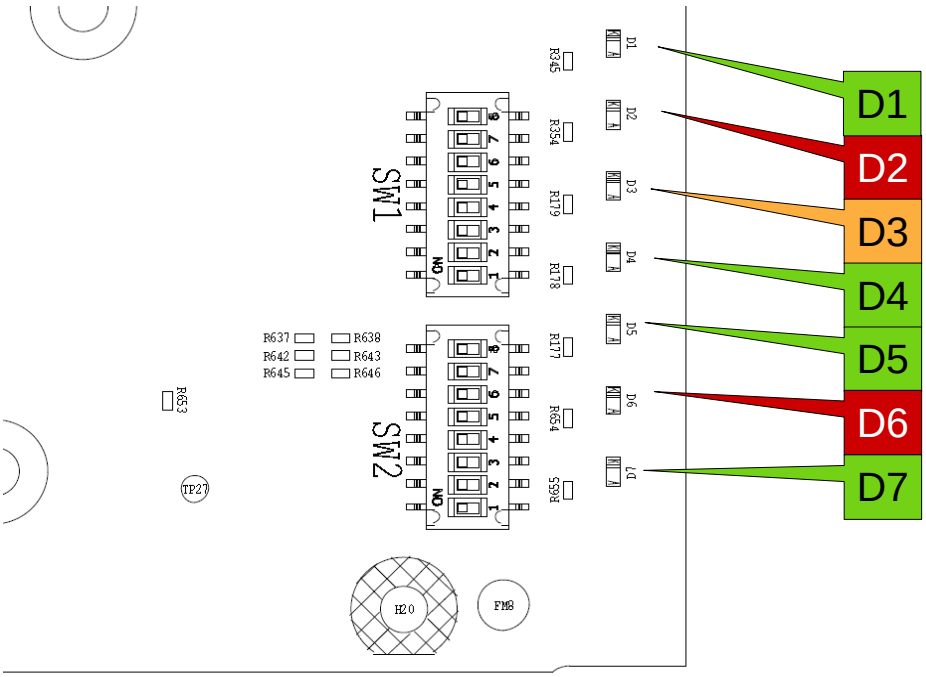

Figure 3 : LED and Switch Locations

Comp. Ref.	Function	ON State	Off State
D7 (Green)	System Monitor Status	See Table 30	
D6 (Red)	System Monitor Status	See Table 30	
D1 (Green)	ACAP (PL) Done	PL is configured	PL is not configured
D3 (Amber)	VPX JTAG STATUS	JTAG chain Connected to VPX P0	JTAG chain isolated from VPX P0
D2 (Red)	PS Error	PS Error	Normal Operation

Table 7 : Status LED Definitions

There also are two user defined LEDs available:

Comp. Ref.	ACAP Pin	Bank	Operation
D5 (Green)	K35	PL Bank 306	Logic low = LED ON
D4 (Green)	K36	PL Bank 306	Logic low = LED ON

Table 8 : User Defined LEDs

4.2 VPX P0 Interface

4.2.1 SYSRESET#

SYSRESET# is an active low input from the system controller

SYSRESET# is connected to the ACAP PL side on Bank 306 (Pin M37)(LVCMOS33)

SYSRESET# is connected to the ACAP PS side PCIe reset pins, LPD_MIO18 and LPD_MIO19 on Bank 502 (Pins F35 and G35)

4.2.2 AUXCLK

Auxiliary Clock. In OpenVPX this clock line can be used for 1PPS synchronization signaling and is an INPUT to the ACAP at Bank306 pin L34 (LVCMOS33).

4.2.3 REFCLK

Reference Clock. This clock is an input to the onboard clock distribution and generation system. In OpenVPX this 50MHz clock can be used to align all system clocks.

This clock is an INPUT to the ACAP at Bank306 pin L35 (LVCMOS33)

4.3 VPX P2 and P3 GPIO

4.3.1 Single Ended GPIO

The Single Ended GPIO on P2 and P3 are routed to/from ACAP bank 710 and are compatible with 3.3V single ended signals at the VPX connector.

The VCCO of Bank 710 is set to 1.5V.

The ACAP is protected by a level translator that can accept up to 3.3V on the VPX side and level shift down to 1.5V at the ACAP side.

4.4 VPX P4 GPIO

4.4.1 Single Ended GPIO

The Single Ended GPIO on P4 are routed to/from ACAP bank 406 and are compatible with 3.3V single ended signals at the VPX connector.

The VCCO of Bank 406 is set to 3.3V.

The ACAP is protected by a buffer.

4.5 JTAG Interface

4.5.1 On-board Interface

A JTAG boundary scan chain is connected to header J4. This allows the connection of the AMD JTAG cable via adapter board AD-JTAG-ADPT2.

Adapter board AD-JTAG-ADPT2 should be inserted into header J4 through the rear of the board, header J4 is keyed to ensure correct orientation.

The scan chain is shown in Figure JTAG Boundary Scan Chain:

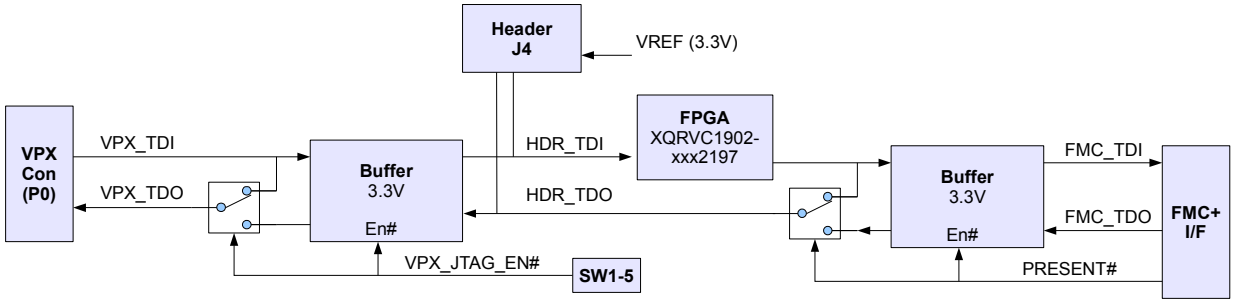

Figure 4 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the VPX backplane (SW1-5 is ON), header J4 should not be used.

4.5.2 VPX Interface

The JTAG interface on the VPX backplane is normally unused. When SW1-5 is OFF (default), all JTAG signals to P0 are left floating.

The JTAG interface can be connected to the VPX Backplane (through level-translators) by switching SW1-5 ON.

4.5.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on J4 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 750mA.

The JTAG signals at the VPX interface use 3.3V signal levels and are connected through buffers to the on-board scan chain.

The JTAG signals at the FMC interface also use 3.3V signal levels and are connected through buffers to FMC boards scan chain.

4.6 Clocks

The **ADM-VA601** board provides a wide variety of clocking options. In addition to the clocks routed from the FMC+ connector, the board has 1 programmable frequency clock source. These clocks can be combined with the ACAP's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADM-VA601** is given in Clocks. A description of each clock follows.

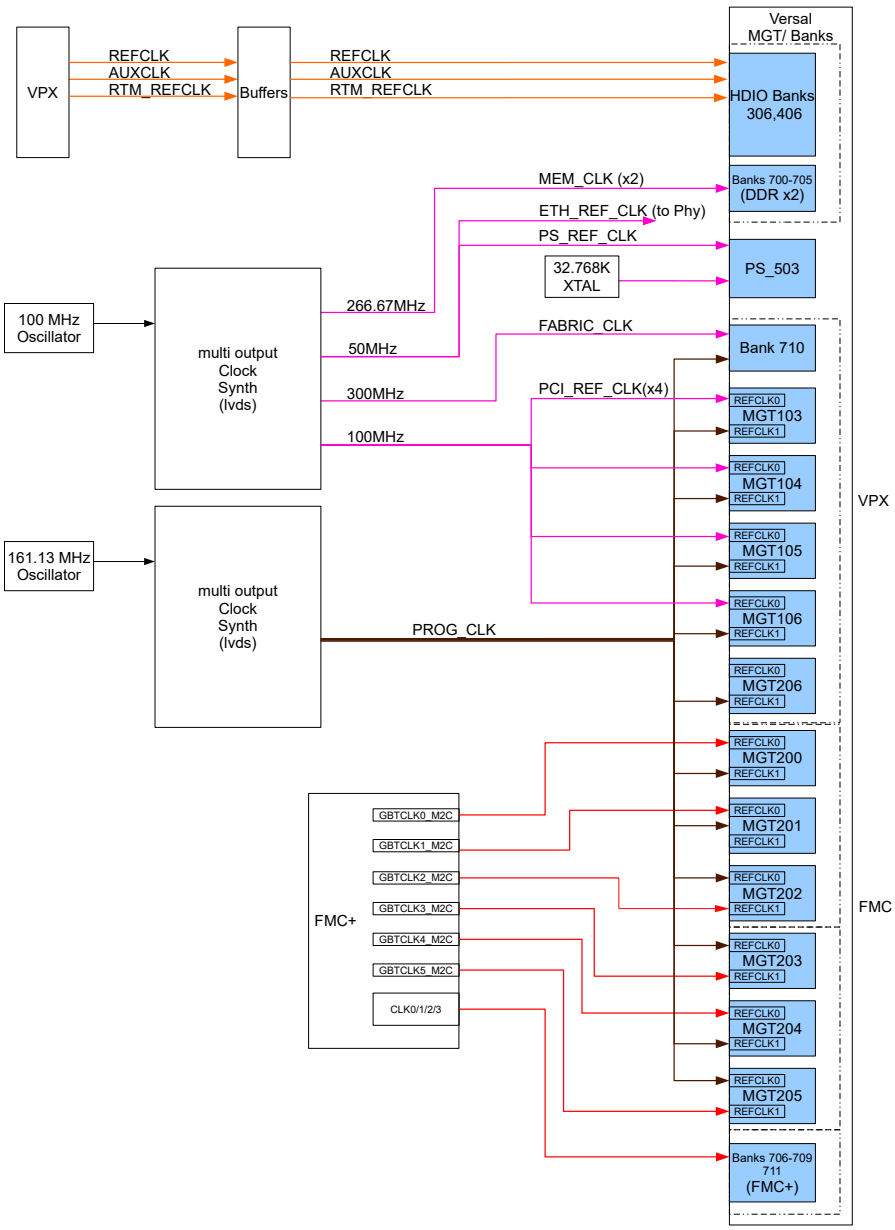

Figure 5 : Clocks

4.6.1 IO Delay Reference Clock (FABRIC_CLK)

The fixed reference clock FABRIC_CLK is a differential LVDS signal.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Use constraints DIFF_TERM_ADV = TERM_100 and IOSTANDARD LVDS15 for this reference clock.

Signal	Frequency	Target ACAP Input	IO Standard	"P" pin	"N" pin
FABRIC_CLK	300 MHz	IO BANK 710	LVDS	AR2	AR1

Table 9 : FABRIC_CLK Connections

4.6.2 DDR4 Memory Reference Clock (MEM_CLK)

The fixed reference clock MEM_CLK is a differential LVDS15 signal.

MEM_CLK is used as the reference clock for the PL DDR memory logic.

Signal	Frequency	DDR Bank	Target ACAP Input	IO Standard	"P" pin	"N" pin
MEM_CLK_0	266.67 MHz	0	IO BANK 701	LVDS15	AM43	AN43
MEM_CLK_1	266.67 MHz	1	IO BANK 704	LVDS15	AY31	BA31

Table 10 : MEM_CLK Connections

4.6.3 Fixed 100MHz PCIe Reference clock PCIE_REFCLK

A fixed 100MHz reference clock is available on the board.

Signal	Frequency	Target ACAP Input	IO Standard	"P" pin	"N" pin
PCIE_REFCLK_0	100 MHz	QUAD 103	LVDS	W39	W40
PCIE_REFCLK_1	100 MHz	QUAD 104	LVDS	R39	R40
PCIE_REFCLK_2	100 MHz	QUAD 105	LVDS	L39	L40
PCIE_REFCLK_3	100 MHz	QUAD 106	LVDS	G39	G40

Table 11 : PCIE_REFCLK Connections

4.6.4 Programmable Clock (PROG_CLK)

There is a programable clock source that is forwarded throughout the ACAP. This clock is programmable through the Alpha Data ADK-VA601 SDK. PROGCLK is generated by a dedicated programmable clock generator IC that offers extremely high frequency resolutions (1ppm increments).

Signal	Frequency	Target ACAP Input	IO Standard	"P" pin	"N" pin
PROGCLK[0]	Variable	IO BANK 710	LVDS	AV9	AW8
PROGCLK[1]	Variable	MGTREFCLK1_103	LVDS	U39	U40
PROGCLK[2]	Variable	MGTREFCLK1_104	LVDS	N39	N40
PROGCLK[3]	Variable	MGTREFCLK1_105	LVDS	J39	J40
PROGCLK[4]	Variable	MGTREFCLK1_106	LVDS	E39	E40
PROGCLK[5]	Variable	MGTREFCLK1_206	LVDS	B15	B14

Table 12 : PROGCLK0 Connections (continued on next page)

Signal	Frequency	Target ACAP Input	IO Standard	"P" pin	"N" pin
PROGCLK[6]	Variable	MGTREFCLK1_200	LVDS	AD11	AD10
PROGCLK[7]	Variable	MGTREFCLK1_201	LVDS	M15	M14
PROGCLK[8]	Variable	MGTREFCLK0_202	LVDS	L13	L12
PROGCLK[9]	Variable	MGTREFCLK0_203	LVDS	J13	J12
PROGCLK[10]	Variable	MGTREFCLK1_204	LVDS	F15	F14
PROGCLK[11]	Variable	MGTREFCLK1_205	LVDS	E13	E12

Table 12 : PROGCLK0 Connections

Note: PROGCLK[11:0] are all buffered copies of the same clock signal. The default (factory set) frequency of PROGCLK = 161.1328MHz.

4.6.5 Module to Carrier Global Clocks (CLK_M2C)

A connected FMC+ board can generate a number of differential Global clocks (as per the FMC standard). They each connect to an global clock input on the ACAP.

Signal	Frequency	ACAP Input	IO Standard	"P" pin	"N" pin
CLK_M2C_0	Variable	Bank 706	LVDS	BA24	BB24
CLK_M2C_1	Variable	Bank 708	LVDS	AY13	BA12
CLK_M2C_2	Variable	Bank 706	LVDS	BC23	BD22
CLK_M2C_3	Variable	Bank 706	LVDS	AV23	AW23

Table 13 : CLK_M2C Connections

4.6.6 Module to Carrier MGTREF Clocks (GBTCLK_M2C)

A connected FMC board can generate a number of differential MGT Reference clocks (as per the FMC standard) . They each connect to an MGTREFCLK input on the ACAP.

Signal	Frequency	ACAP Input	IO Standard	"P" pin	"N" pin
GBTCLK_0_M2C	Variable	MGTREFCLK_200	LVDS	AF11	AF10
GBTCLK_1_M2C	Variable	MGTREFCLK_201	LVDS	AB11	AB10
GBTCLK_2_M2C	Variable	MGTREFCLK_202	LVDS	K15	K14
GBTCLK_3_M2C	Variable	MGTREFCLK_203	LVDS	H15	H14
GBTCLK_4_M2C	Variable	MGTREFCLK_204	LVDS	G13	G12
GBTCLK_5_M2C	Variable	MGTREFCLK_205	LVDS	D15	D14

Table 14 : GCLK_M2C Connections

4.6.7 PS_REFCLK

The PS reference clock is an independent 50.0MHz reference clock. This is the master clock of the PS side of the ACAP.

Signal	Frequency	ACAP Input	IO Standard	pin
PS_REFCLK	50MHz	PS_REF_CLK (Bank 503)	LVCMOS33	AE32

Table 15 : PS_REFCLK Connection

4.6.8 ETH_REF_CLK

The Ethernet reference clock is a 50.0MHz reference clock that is required by the on board Ethernet Phy.

Signal	Frequency	Phy Input	IO Standard	pin
ETH_REF_CLK	50MHz	XTAL1	LVCMOS33	63

Table 16 : ETH_REF_CLK Connection

4.7 Resets

The ACAP PS can be reset via switch SW2-5.

Switch	Reset Type	Effect
SW2-5	Power on Reset (PS_POR_B pin)	Clears all logic. Mode pins sampled (i.e. reconfigures hardware). Reboots ACAP.

Table 17 : Reset Switches

4.8 ACAP PS Block

4.8.1 Boot Modes

MODE3 (SW2-4)	MODE2 (SW2-3)	MODE1 (SW2-2)	MODE0 (SW2-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24 bit addressing)
ON	ON	OFF	ON	Quad SPI (32 bit addressing)
ON	OFF	ON	OFF	SD Flash - SD 2.0

Table 18 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

4.8.2 Configuration Daughter Board

The ADM-VA601 board has a socket (J2) that allows custom configuration boards to be used.

The ADM-SDEV-FL1 configuration daughter board is supplied with the ADM-VA601 board as part of the ADK-VA601 development kit.

The ADM-SDEV-FL1 configuration daughter board should be inserted into connector J2.

The ADM-SDEV-FL1 configuration daughter board contains QSPI flash memory which can be used to configure the ACAP device.

4.8.2.1 QSPI Flash Memory

The ADM-SDEV-FL1 board has 2x 1Gb (128MB) quad-QSPI Flash devices. These can be interfaced in x1,x2,x4 or x8 mode.

See MIO Map

4.8.2.2 MicroSD Card

The ADM-VA601 board has a MicroSD card socket (SD 2.0 standard at 3.3V).

See MIO Map

4.8.3 SMAP Interface

The entire 32bit SMAP interface is passed out to the VPX P4 connector via bidirectional buffers.

If the SMAP interface is not required then these pins may be used as MIO GPIO.

See MIO Map

4.8.4 Ethernet RGMII Interface

The Gigabit Ethernet Manager (GEM0) is interfaced with a Microchip VSC8541 phy to provide 10/100/1000 Base-T Ethernet to the ACAP. This interface is accessible at the VPX P3 connector.

The Gigabit Ethernet Manager (GEM0) connects to the phy via RGMII and MDIO interfaces.

See MIO Map

4.8.5 UART interface

The UART0 interface is routed through to the VPX P3 connector. See MIO Map

The UART0 interface operates at 3.3V switching levels.

See MIO Map

4.9 ACAP PL Side

4.9.1 I/O Bank Voltages

The ACAP IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in PL ACAP IO Banks.

IO Banks	Voltage	Purpose
706, 707, 708	FMC_VADJ	FMC+ GPIO - LA and HA
709	FMC_VIO_B	FMC+ GPIO - HB
710	1.5V	VPX P2 and P3 SE GPIO
700, 701, 702	1.2V	DDR4 Bank0
703, 704, 705	1.2V	DDR4 Bank1
306	3.3V	Spacewire and VPX Clocks
406	3.3V	CAN and VPX P4 3.3V GPIO
711	FMC_VADJ	Unused

Table 19 : PL ACAP IO Banks

4.9.2 PL MGT Links

There are a total of 44 Multi-Gigabit Transceiver (MGT) links connected to the ACAP. These are connected as follows:

Links	Banks	Width	Max Rate	Connection
FMC_HSSIO(23:0)	200, 201, 202, 203, 204, 205	24	32.75Gbps	GTY links to FMC+ Socket (J3)
VPX_P1_HSSIO (15:0)	103, 104, 105, 106	16	16Gbps	VPX P1 Connector Data Planes (4 fat pipes)
VPX_P2_HSSIO(3:0)	206	4	16Gbps	SpaceFibre in VPX P2 Connector User Defined Area

Table 20 : PL MGT Links

4.9.3 FMC+ GPIO Interface

The FMC+ Connector (J1) has GPIO connections arranged as follows:

Group	ACAP Bank	Name	Function
LA_0	707	LA(16:2)	15 diff. Pairs / 30 single-ended
		LA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
n/a	n/a	LA (24:19)	6 diff. Pairs / 12 single-ended
n/a	n/a	LA_CC (18:17)	2x Regional Clocks / GPIO pairs / 4 single-ended
LA_1	706	LA(33:25)	9 diff. Pairs / 18 single-ended
		HA(16:2)	15 diff. Pairs / 30 single-ended
n/a	n/a	HA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
n/a	n/a	HA(23:18)	6 diff. Pairs / 12 single-ended
n/a	n/a	HA_CC (17)	Regional Clock / GPIO pair / 2 single-ended
HB_0	709	HB(5:1)	5 diff. Pairs / 10 single-ended
		HB(16:7)	10 diff. Pairs / 20 single-ended
		HB(21:18)	4 diff. Pairs / 8 single-ended
		HB_CC (0)	Regional Clock / GPIO pair / 2 single-ended
		HB_CC (6)	Regional Clock / GPIO pair / 2 single-ended
		HB_CC (17)	Regional Clock / GPIO pair / 2 single-ended

Table 21 : FMC+ Groups

4.9.4 FMC VADJ Power Supply

The ADM-VA601 board is fully compliant with the VITA 57.1 standard. This means that any FMC card that is used with the board should have an EEPROM on board programmed according to the IPMI format defined in the VITA 57.1 FMC specification.

The IPMI specification notes that an FMC board should use a 2K EEPROM which is compatible with 24C02 devices. This EEPROM must be available to be queried at power on in order that the FMC slot VADJ voltage can then be set up and turned on.

If this specification is not followed, the VADJ voltage to the FMC slot in question will not automatically power up (it will correctly remain at 0V).

Note:
In the event that this EEPROM is not present on the FMC board, there is an EEPROM on the ADM-VA601 that can be used to configure the FMC VADJ power supply instead (see switch SW2-6). The use of this alternative method is not recommended practice.

4.9.5 CAN interfaces

Two CAN interfaces are routed to Rad hard transceiver chips on the board.

Signal	Bank	Type	IO Standard
CAN0_TX	406	EMIO	LVCMOS33
CAN0_RX	406	EMIO	LVCMOS33
CAN1_TX	502	MIO	LVCMOS33
CAN1_RX	502	MIO	LVCMOS33

Table 22 : CAN PL side connections

The other sides of the CAN transceivers are routed out to the VPX P3 connector.

4.9.6 VPX P2 GPIO Interface

The P2 VPX Connector has GPIO connections arranged as a single byte wide lane as follows:

Group	ACAP Bank	Name	Function
GPIO_0	710	GPIO(7:0)	8 single-ended

Table 23 : VPX P2 GPIO Groups

4.9.7 VPX P3 GPIO Interface

The P3 VPX Connector has GPIO connections arranged into 3 byte wide lanes as follows:

Group	ACAP Bank	Name	Function
GPIO_1	710	GPIO(31:8)	24 single-ended

Table 24 : VPX P2 GPIO Groups

4.9.8 VPX P4 GPIO Interface

The P4 VPX Connector has GPIO connections arranged as follows:

Group	ACAP Bank	Name	Function
GPIO_2	406	GPIOB(7:0)	8 single-ended IO
MIO	501	MIO(43:40)	4 single-ended inputs
MIO	501	MIO(39:36)	4 single-ended outputs

Table 25 : VPX P2 GPIO Groups

4.9.9 VPX GPIO Buffers

The VPX Connector GPIO connections are buffered by byte wide SN54SLC8T245-SEP bidirectional buffers.

Each byte lane buffer has a dedicated output enable pin and a direct control pin.

Name	Function
OE_L	Output Enable : 0=ENABLED 1=DISABLED
DIR	Direction Control : 0=INPUT 1=OUTPUT

Table 26 : Buffer Pins

4.9.10 DDR4 Memory

Two banks of DDR4 SDRAM memory are soldered down to the board. The available density of the memory is 8GB/per bank, 16GB total. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 2133 MT/s.

Memory solutions are available from AMD (See AMD PG313 Versal ACAP Programmable Network on Chip and Integrated Memory Controller v1.0). All pin location information is included in DDR4 Pinout Table.

The components used are Teledyne e2v DDR4PT08G72AZR1B or equivalent.

4.9.11 Temperature Sensor

A TMP9R01-SEP temperature sensor is connected to the PL side of the ACAP.

Signal	Bank	IO Standard	pin
PL_TEMP_SDA	406	LVCMOS33	H17
PL_TEMP_SCL	406	LVCMOS33	H18

Table 27 : PL Side TMP422-EP Connections

4.10 System Monitoring

The **VA601** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using a Vorago VA41630 microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the ACAP, where they can be stored in blockram.

The following voltage rails and temperatures are monitored by the microcontroller:

Monitor	*Purpose*
12V0_VPX	12V Board Input Supply Voltage
5V0_DIG	5V Board Supply Voltage
3V3_DIG	Board Supply Voltage
12V0	12V Board Input Supply Current
3V3_CLK	3.3V IO Supply Voltage
5V0_DIG2	5V Secondary Board Supply Voltage
1V5_DIG	1.5V Board Supply Voltage
1V2_DIG	1.2V DDR Supply Voltage
VCC_INT	0.8V ACAP Core Voltage
FMC_VADJ	Variable FMC IO Supply Voltage
Temp(1)	microcontroller internal temperature

Table 28 : Voltage and Temperature Monitors (in microcontroller) (continued on next page)

Monitor	*Purpose*
Temp(4..2)	TMP9R01-SEP internal temperatures (3 devices)
Temp(5)	ACAP on-die temperature (measured by TMP422-EP)
Temp(10..6)	pcb temperatures (5 different points - measured by TMP422-EP devices)

Table 28 : Voltage and Temperature Monitors (in microcontroller)

4.10.1 Automatic Temperature Monitoring

The system monitor checks that the board and ACAP are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the ACAP by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	Target ACAP				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Extended	-5°C	+5°C	+95°C	+105°C	-5°C	+5°C	+80°C	+90°C
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C
Military	-60°C	-50°C	+140°C	+170°C	-60°C	-50°C	+125°C	+135°C

Table 29 : Temperature Limits

4.10.2 System Monitor Status LEDs

LEDs D7 (Green) and D6 (Red) indicate the microcontroller status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	ACAP configuration cleared to protect board

Table 30 : System Monitor Status LEDs

4.11 FMC Interface and Front-Panel I/O

The FMC+ interface provides a high-performance and flexible front-panel interface through a range of interchangeable, industry standard IO modules which connect at receptacle J3.

The FMC+ interface adheres to VITA 57.4. The ADM-VA601 utilizes all possible FMC+ connectivity. This includes all GPIO, all MGT links, and all clock capable IO.

FMC I2C signal (SCL and SDA at C30 and C31) are connected to the system monitor microcontroller. They are used to determine operating voltage during startup and are not accesable to the user.

The FMC Present signal (PRSNT_M2C_L at connector pin H2) is connected to the system monitor microcontroller.

Note:
The ADM-VA601 supports only 1.5V and lower VADJ Voltages.

4.12 Configuration

There are three main ways of configuring the ACAP on the ADM-VA601:

- From QSPI Flash memory, at power-on, as described in Section 4.12.1
- From uSD Flash memory, at power-on, as described in Section 4.12.2
- Using USB cable connected at either USB port Section 4.12.3

4.12.1 Configuration From QSPI Flash Memory

The ACAP can be automatically configured at power-on from two 1 Gbit QSPI flash memory devices configured as an x8 dual parallel SPI device (2x Micron part number MT25QL01GBBB8E12).

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 4.8.1. If the mode is set to QSPI24 or QSPI32, the ACAP will search on the header of the binary that has been flashed into the card. This normally results in SPIx8 configuration.

4.12.1.1 Building and Programming QSPI Configuration Images

Example Vivado projects(.xpr format) are available in the downloads area for the ADK-VA601. Access should be requested via email to: **support@alpha-data.com**

Below are described the steps to do QSPI Flash programming.

- Connect the ADM-VA601 to a VPX system
- Ensure ADM-VA601 switches SW2-1, SW2-2, SW2-3, SW2-4 are all ON (see Switch Definitions)
- Set ADM-VA601 SW1-5 to ON to switch the JTAG chain through to the ADM-VA600-RTM (see Switch Definitions)
- Connect the download cable between the test PC and the JTAG programming header on the ADM-VA600-RTM (J29)

The flash programming commands are run via Vivado as follows:

- Open Vivado -> Open Project(select .xpr file) -> Select HW Manager -> Open Target -> Auto Connect
- Right click on xcvc1902_1 -> Add Configuration Memory Device -> search for 'cfgmem-qspi-x8-dual_parallel', selecting it -> click OK
- A message asking the user to configure the device now will pop up. Click OK accepting it
- Now, copy the path to the PDI image in the 'Initialization PDI' field, and click OK. This will program the QSPI Flash with the example design that you have opened. If you have a .BIN file instead, use the path for that binary file and leave the other fields as are

If you followed the previous steps, the ACAP should have been correctly configured. To verify this, power off the ADM-VA601, set switches SW2-1, SW2-3, SW2-4 ON and SW2-2 OFF. Then power up the ADM-VA601. Both the DONE_L and STAT_0 LEDs should illuminate after a few seconds(see LED Definitions)

4.12.2 Configuration From uSD Flash Memory

The ACAP can be automatically configured at power-on from the Micro Secure Digital card (uSD) in the centre of the board.

The ADM-VA601 is shipped with a simple bitstream. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 4.8.1. Alpha Data ships these cards set to the uSD boot mode by default.

4.12.2.1 Building and Programming uSD Configuration Images

Find below the steps to get a bootable image file(BOOT.BIN) from your implemented example design,

- Prepare the uSD card by formatting it as a whole FAT partition.

- Find the generated PDI file of your design(implementation folder of the project).
- Copy the .pdi to FAT32 SD card and rename it to BOOT.bin

The uSD card is now ready to be booted from. It can be inserted in the ADM-VA601 with the appropriate boot switch setting. The example design will be programmed into the ACAP automatically at boot.

4.12.3 Configuration via JTAG

An AMD-Xilinx download Cable may be attached to the JTAG download header on the ADM-VA600-RTM. This permits the ACAP to be reconfigured using the Xilinx Vivado Hardware Manager. The device will be automatically recognized in Vivado Hardware Manager and Vitis.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908

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Appendix A: P1 Pin Assignments

Appendix A.1: Data Plane 1 (P1 Wafers 1-4)

Signal	VPX P1	ACAP		ACAP	VPX P1	Signal
P1_TX0_N	E1	AB42	|	AB47	B1	P1_RX0_N
P1_TX0_P	D1	AB41	|	AB46	A1	P1_RX0_P
P1_TX1_N	F2	Y42	|	AA45	C2	P1_RX1_N
P1_TX1_P	E2	Y41	|	AA44	B2	P1_RX1_P
P1_TX2_N	E3	V42	|	Y47	B3	P1_RX2_N
P1_TX2_P	D3	V41	|	Y46	A3	P1_RX2_P
P1_TX3_N	F4	U44	|	W45	C4	P1_RX3_N
P1_TX3_P	E4	U43	|	W44	B4	P1_RX3_P

Table 31 : Data Plane 1 (P1 Wafers 1-4)

Appendix A.2: Data Plane 2 (P1 Wafers 5-8)

Signal	VPX P1	ACAP		ACAP	VPX P1	Signal
P1_TX4_N	E5	T42	|	V47	B5	P1_RX4_N
P1_TX4_P	D5	T41	|	V46	A5	P1_RX4_P
P1_TX5_N	F6	R44	|	T47	C6	P1_RX5_N
P1_TX5_P	E6	R43	|	T46	B6	P1_RX5_P
P1_TX6_N	E7	P42	|	P47	B7	P1_RX6_N
P1_TX6_P	D7	P41	|	P46	A7	P1_RX6_P
P1_TX7_N	F8	M42	|	N45	C8	P1_RX7_N
P1_TX7_P	E8	M41	|	N44	B8	P1_RX7_P

Table 32 : Data Plane 2 (P1 Wafers 5-8)

Appendix A.3: Data Plane 3 (P1 Wafers 9-12)

Signal	VPX P1	ACAP		ACAP	VPX P1	Signal
P1_TX8_N	E9	K42	|	M47	B9	P1_RX8_N
P1_TX8_P	D9	K41	|	M46	A9	P1_RX8_P
P1_TX9_N	F10	J44	|	L45	C10	P1_RX9_N
P1_TX9_P	E10	J43	|	L44	B10	P1_RX9_P
P1_TX10_N	E11	H42	|	K47	B11	P1_RX10_N
P1_TX10_P	D11	H41	|	K46	A11	P1_RX10_P
P1_TX11_N	F12	G44	|	H47	C12	P1_RX11_N
P1_TX11_P	E12	G43	|	H46	B12	P1_RX11_P

Table 33 : Data Plane 3 (P1 Wafers 9-12)

Appendix A.4: Data Plane 4 (P1 Wafers 13-16)

Signal	VPX P1	ACAP		ACAP	VPX P1	Signal
P1_TX12_N	E13	F42	|	F47	B13	P1_RX12_N
P1_TX12_P	D13	F41	|	F46	A13	P1_RX12_P
P1_TX13_N	F14	D42	|	E45	C14	P1_RX13_N
P1_TX13_P	E14	D41	|	E44	B14	P1_RX13_P
P1_TX14_N	E15	B42	|	D47	B15	P1_RX14_N
P1_TX14_P	D15	B41	|	D46	A15	P1_RX14_P
P1_TX15_N	F16	A44	|	C45	C16	P1_RX15_N
P1_TX15_P	E16	A43	|	C44	B16	P1_RX15_P

Table 34 : Data Plane 4 (P1 Wafers 13-16)

Appendix B: P2 Pin Assignments

Appendix B.1: GPIO (P2 Row G)

Signal	VPX P2	ACAP		ACAP	VPX P2	Signal
GPIO<0>	AW2	AK14	|	AN10	AT3	GPIO<4>
GPIO<1>	AV2	AJ14	|	AM10	AU3	GPIO<5>
GPIO<2>	AW3	AN13	|	AN11	AW5	GPIO<6>
GPIO<3>	AV3	AM13	|	AM11	AW4	GPIO<7>
OE_L<0>	-	AT2	|	AT1	-	DIR<1>

Table 35 : GPIO (P2 Row G)

Appendix B.2: MGT Pins (P2 Wafers 1-4)

Signal	VPX P2	ACAP		ACAP	VPX P2	Signal
P2_TX0_N	E1	C8	|	AM3	D1	P2_RX0_N
P2_TX0_P	D1	C9	|	AM4	D2	P2_RX0_P
P2_TX1_N	F2	B10	|	AL1	D5	P2_RX1_N
P2_TX1_P	E2	B11	|	AL2	D6	P2_RX1_P
P2_TX2_N	E3	A8	|	AK3	C3	P2_RX2_N
P2_TX2_P	D3	A9	|	AK4	C4	P2_RX2_P
P2_TX3_N	F4	A12	|	AJ1	B5	P2_RX3_N
P2_TX3_P	E4	A13	|	AJ2	B6	P2_RX3_P

Table 36 : MGT (P2 Wafers 1-4)

Appendix C: P3 Pin Assignments

Appendix C.1: Ethernet Pins (P3 Wafers 1-3)

Signal	VPX P3		VPX P3	Signal
ETH_OUT_0_N	B1	|	C2	ETH_OUT_2_N
ETH_OUT_0_P	A1	|	B2	ETH_OUT_2_P
ETH_OUT_1_N	E1	|	F2	ETH_OUT_3_N
ETH_OUT_1_P	D1	|	E2	ETH_OUT_3_P
ETH_LED0	A3	|	B3	ETH_LED1

Table 37 : Ethernet (P3 Wafers 1-3)

Appendix C.2: Serial Interfaces (P3 Wafers 3-4)

Signal	VPX P3	Notes
UART0_RXD	C4	UART0 RX
UART0_TXD	B4	UART0 TX
CAN0H	D3	CAN BUS0 H
CAN0L	E3	CAN BUS0 L
CAN1H	D13	CAN BUS1 H
CAN1L	E13	CAN BUS1 L

Table 38 : Serial Interfaces (P3 Wafers 3-4)

Appendix C.3: GPIO (P3 Wafers 5-8)

Signal	VPX P3	ACAP		ACAP	VPX P3	Signal
GPIO<8>	G1	AV1	|	AV6	C6	GPIO<20>
GPIO<9>	G3	AU1	|	AU6	E6	GPIO<21>
GPIO<10>	G5	AN3	|	AY10	F6	GPIO<22>
GPIO<11>	G7	AM3	|	AY9	A7	GPIO<23>
GPIO<12>	G9	AT4	|	AP10	B7	GPIO<24>
GPIO<13>	G11	AR4	|	AN10	D7	GPIO<25>
GPIO<14>	G13	AP2	|	AP8	E7	GPIO<26>
GPIO<15>	G15	AN1	|	AR7	B8	GPIO<27>
GPIO<16>	B5	AW7	|	AP9	C8	GPIO<28>
GPIO<17>	D5	AV7	|	AR9	E8	GPIO<29>
GPIO<18>	E5	AU8	|	AN8	F8	GPIO<30>
GPIO<19>	B6	AU9	|	AP7	A9	GPIO<31>
OE_L<1>	-	AN2	|	AM1	-	DIR<1>

Table 39 : GPIO (P3 Wafers 5-8) (continued on next page)

Signal	VPX P3	ACAP		ACAP	VPX P3	Signal
OE_L<2>	-	AV10		AW9	-	DIR<2>
OE_L<3>	-	AT8		AT7	-	DIR<3>

Table 39 : GPIO (P3 Wafers 5-8)

Appendix C.4: P3 Misc

Signal	VPX P3	Notes
VCC_EFUSE	D9	EFUSE / VBATT VOLTAGE IN
MIO13_IN	A5	MIO13 GPIO IN - FACTORY USE ONLY
MSP_MON_RX	F4	MSP UART RX - FACTORY USE ONLY
MSP_MON_TX	E4	MSP UART TX - FACTORY USE ONLY
TEST_MODE_N	B9	FACTORY USE ONLY

Table 40 : P3 Misc

Appendix D: P4 Pin Assignments

Appendix D.1: SMAP Interface (P4 Wafers 1-5)

Signal	VPX P4
SMAP_BUSY_OUT	D1
SMAP_CLK_IN	E1
SMAP_CS_B_IN	B1
SMAP_OUT_D<0>	B2
SMAP_OUT_D<1>	C2
SMAP_OUT_D<2>	E2
SMAP_OUT_D<3>	F2
SMAP_OUT_D<4>	A3
SMAP_OUT_D<5>	B3
SMAP_OUT_D<6>	D3
SMAP_OUT_D<7>	E3
SMAP_OUT_D<8>	B4
SMAP_OUT_D<9>	C4
SMAP_OUT_D<10>	E4
SMAP_OUT_D<11>	F4
SMAP_OUT_D<12>	A5
SMAP_OUT_D<13>	B5
SMAP_OUT_D<14>	D5
SMAP_OUT_D<15>	E5
SMAP_RDWR_B_IN	A1

Table 41 : SMAP Interface(P4 Wafers 1-5)

Appendix D.2: SpaceWire Interface (P4 Wafers 13-16)

Signal (DIFF)	VPX P4	ACAP (SE)		ACAP (SE)	VPX P4	Signal (DIFF)
SPW01_DOUT_N	F16	M36	|	L37	C16	SPW01_DIN_N
SPW01_DOUT_P	E16	-	|	-	B16	SPW01_DIN_P
SPW02_DOUT_N	F14	L33	|	N34	C14	SPW02_DIN_N
SPW02_DOUT_P	E14	-	|	-	B14	SPW02_DIN_P
SPW01_SOUT_N	E15	K33	|	M34	B15	SPW01_SIN_N
SPW01_SOUT_P	D15	-	|	-	A15	SPW01_SIN_P
SPW02_SOUT_N	E13	K37	|	M35	B13	SPW02_SIN_N
SPW02_SOUT_P	D13	-	|	-	A13	SPW02_SIN_P

Table 42 : SpaceWire Interface (P4 Wafers 13-16)

Appendix D.3: MIO (P4 Wafers 6-7)

Signal	Dir	VPX P4	ACAP	|	ACAP	VPX P4	Dir	Signal
MIO<36>	Out	B6	B19	|	C19	C6	Out	MIO<37>
MIO<38>	Out	E6	D19	|	F19	F6	Out	MIO<39>
MIO<40>	In	A7	G19	|	F18	B7	In	MIO<41>
MIO<42>	In	D7	E18	|	D18	E7	In	MIO<43>

Table 43 : MIO (P4 Wafers 6-7)

Appendix D.4: GPIOB (P4 Row G)

Signal	VPX P4	ACAP	|	ACAP	VPX P4	Signal
GPIOB<0>	G1	M17	|	L18	G9	GPIOB<4>
GPIOB<1>	G3	L17	|	K17	G11	GPIOB<5>
GPIOB<2>	G5	M19	|	L20	G13	GPIOB<6>
GPIOB<3>	G7	L19	|	L21	G15	GPIOB<7>
OEB_L	-	M20	|	M21	-	DIRB

Table 44 : GPIOB (P4 Row G)

Appendix D.5: P4 Misc

Signal	VPX P4	Notes
RTM_REFCLK_N	C10	LVDS DIFF REFCLK FROM RTM to ACAP SE Pin L35
RTM_REFCLK_P	B10	-

Table 45 : P4 Misc

Appendix E: FMC Pin Assignments

Appendix E.1: GPIO Pins

Signal	FMC (J1)	ACAP		ACAP	FMC (J1)	Signal
LA00_CC_N	G7	AY18	|	AV13	F5	HA00_CC_N
LA00_CC_P	G6	AW19	|	AU13	F4	HA00_CC_P
LA01_CC_N	D9	AP18	|	BD13	E3	HA01_CC_N
LA01_CC_P	D8	AP19	|	BC13	E2	HA01_CC_P
LA02_N	H8	AM20	|	AU15	K8	HA02_N
LA02_P	H7	AM21	|	AT14	K7	HA02_P
LA03_N	G10	AN19	|	AN13	J7	HA03_N
LA03_P	G9	AN20	|	AP12	J6	HA03_P
LA04_N	H11	BG19	|	AT11	F8	HA04_N
LA04_P	H10	BF19	|	AR11	F7	HA04_P
LA05_N	D12	AM17	|	AR12	E7	HA05_N
LA05_P	D11	AL16	|	AP11	E6	HA05_P
LA06_N	C11	AR20	|	AT13	K11	HA06_N
LA06_P	C10	AT20	|	AR14	K10	HA06_P
LA07_N	H14	AV18	|	AU11	J10	HA07_N
LA07_P	H13	AV19	|	AU12	J9	HA07_P
LA08_N	G13	AU16	|	AR15	F11	HA08_N
LA08_P	G12	AT17	|	AP15	F10	HA08_P
LA09_N	D15	AN17	|	AP13	E10	HA09_N
LA09_P	D14	AM18	|	AN14	E9	HA09_P
LA10_N	C15	AR17	|	AV14	K14	HA10_N
LA10_P	C14	AT16	|	AV15	K13	HA10_P
LA11_N	H17	AP16	|	BC11	J13	HA11_N
LA11_P	H16	AN16	|	BB11	J12	HA11_P
LA12_N	G16	AT19	|	AW13	F14	HA12_N
LA12_P	G15	AR18	|	AW12	F13	HA12_P
LA13_N	D18	AU19	|	AW11	E13	HA13_N
LA13_P	D17	AU20	|	AV11	E12	HA13_P
LA14_N	C19	AV17	|	BF12	J16	HA14_N
LA14_P	C18	AU17	|	BE11	J15	HA14_P
LA15_N	H20	BB19	|	BE14	F17	HA15_N
LA15_P	H19	BB20	|	BE15	F16	HA15_P

Table 46 : GPIO Pins **(continued on next page)**

Signal	FMC (J1)	ACAP		ACAP	FMC (J1)	Signal
LA16_N	G19	AY19	|	BD12	E16	HA16_N
LA16_P	G18	AW20	|	BC12	E15	HA16_P
LA17_CC_N	D21	BC16	|	BB13	K17	HA17_CC_N
LA17_CC_P	D20	BB16	|	BB14	K16	HA17_CC_P
LA18_CC_N	C23	BD17	|	BC15	J19	HA18_N
LA18_CC_P	C22	BE17	|	BB15	J18	HA18_P
LA19_N	H23	BA16	|	BD14	F20	HA19_N
LA19_P	H22	BA17	|	BD15	F19	HA19_P
LA20_N	G22	BA19	|	BG11	E19	HA20_N
LA20_P	G21	BA20	|	BF11	E18	HA20_P
LA21_N	H26	BD19	|	BF13	K20	HA21_N
LA21_P	H25	BE19	|	BE12	K19	HA21_P
LA22_N	G25	BC17	|	BG13	J22	HA22_N
LA22_P	G24	BB18	|	BF14	J21	HA22_P
LA23_N	D24	BD18	|	BG14	K23	HA23_N
LA23_P	D23	BC18	|	BG15	K22	HA23_P
LA24_N	H29	BG16	|	BB4	K26	HB00_CC_N
LA24_P	H28	BF16	|	BB3	K25	HB00_CC_P
LA25_N	G28	BE20	|	AY1	J25	HB01_N
LA25_P	G27	BE21	|	AY2	J24	HB01_P
LA26_N	D27	BF17	|	BA2	F23	HB02_N
LA26_P	D26	BE16	|	BA3	F22	HB02_P
LA27_N	C27	BE24	|	AY4	E22	HB03_N
LA27_P	C26	BE25	|	AY5	E21	HB03_P
LA28_N	H32	BF22	|	BB1	F26	HB04_N
LA28_P	H31	BG21	|	BA1	F25	HB04_P
LA29_N	G31	BE22	|	BA4	E25	HB05_N
LA29_P	G30	BF23	|	BB5	E24	HB05_P
LA30_N	H35	BG20	|	BC3	K29	HB06_CC_N
LA30_P	H34	BF21	|	BD4	K28	HB06_CC_P
LA31_N	G34	BG18	|	BD9	J28	HB07_N
LA31_P	G33	BF18	|	BD10	J27	HB07_P
LA32_N	H38	BG24	|	BE4	F29	HB08_N
LA32_P	H37	BG25	|	BF4	F28	HB08_P
LA33_N	G37	BG23	|	BD2	E28	HB09_N
LA33_P	G36	BF24	|	BD3	E27	HB09_P

Table 46 : GPIO Pins (continued on next page)

Signal	FMC (J1)	ACAP		ACAP	FMC (J1)	Signal
HB16_N	F35	BC7	|	BC1	K32	HB10_N
HB16_P	F34	BC8	|	BC2	K31	HB10_P
HB17_CC_N	K38	BC6	|	BE10	J31	HB11_N
HB17_CC_P	K37	BD7	|	BE9	J30	HB11_P
HB18_N	J37	BG8	|	AY6	F32	HB12_N
HB18_P	J36	BG9	|	AY7	F31	HB12_P
HB19_N	E34	BA8	|	BB9	E31	HB13_N
HB19_P	E33	BB8	|	BC10	E30	HB13_P
HB20_N	F38	BF7	|	BG4	K35	HB14_N
HB20_P	F37	BF8	|	BG5	K34	HB14_P
HB21_N	E37	BE7	|	BE2	J34	HB15_N
HB21_P	E36	BD8	|	BF3	J33	HB15_P
FMC_CLK_DIR	B1	G20	|	-	-	-

Table 46 : GPIO Pins

Appendix E.2: Clock Pins

Signal	FMC (J1)	ACAP		ACAP	FMC (J1)	Signal
CLK0_M2C_N	H5	BB24	|	BD22	K5	CLK2_BIDIR_N
CLK0_M2C_P	H4	BA24	|	BC23	K4	CLK2_BIDIR_P
CLK1_M2C_N	G3	BA12	|	AW23	J3	CLK3_BIDIR_N
CLK1_M2C_P	G2	AY13	|	AV23	J2	CLK3_BIDIR_P
GBTCLK0_M2C_N	D5	AF10	|	H14	L9	GBTCLK3_M2C_N
GBTCLK0_M2C_P	D4	AF11	|	H15	L8	GBTCLK3_M2C_P
GBTCLK1_M2C_N	B21	AB10	|	G12	L5	GBTCLK4_M2C_N
GBTCLK1_M2C_P	B20	AB11	|	G13	L4	GBTCLK4_M2C_P
GBTCLK2_M2C_N	L13	K14	|	D14	Z21	GBTCLK5_M2C_N
GBTCLK2_M2C_P	L12	K15	|	D15	Z20	GBTCLK5_M2C_P

Table 47 : Clock Pins

Appendix E.3: MGT Pins

Signal	FMC (J1)	ACAP		ACAP	FMC (J1)	Signal
DP0_M2C_N	C7	AF1	|	AF6	C3	DP0_C2M_N
DP0_M2C_P	C6	AF2	|	AF7	C2	DP0_C2M_P
DP1_M2C_N	A3	AE3	|	AE8	A23	DP1_C2M_N
DP1_M2C_P	A2	AE4	|	AE9	A22	DP1_C2M_P
DP2_M2C_N	A7	AD1	|	AD6	A27	DP2_C2M_N
DP2_M2C_P	A6	AD2	|	AD7	A26	DP2_C2M_P
DP3_M2C_N	A11	AC3	|	AC8	A31	DP3_C2M_N
DP3_M2C_P	A10	AC4	|	AC9	A30	DP3_C2M_P
DP4_M2C_N	A15	AB1	|	AB6	A35	DP4_C2M_N
DP4_M2C_P	A14	AB2	|	AB7	A34	DP4_C2M_P
DP5_M2C_N	A19	AA3	|	AA8	A39	DP5_C2M_N
DP5_M2C_P	A18	AA4	|	AA9	A38	DP5_C2M_P
DP6_M2C_N	B17	Y1	|	Y6	B37	DP6_C2M_N
DP6_M2C_P	B16	Y2	|	Y7	B36	DP6_C2M_P
DP7_M2C_N	B13	W3	|	W8	B33	DP7_C2M_N
DP7_M2C_P	B12	W4	|	W9	B32	DP7_C2M_P
DP8_M2C_N	B9	V1	|	V6	B29	DP8_C2M_N
DP8_M2C_P	B8	V2	|	V7	B28	DP8_C2M_P
DP9_M2C_N	B5	U3	|	U8	B25	DP9_C2M_N
DP9_M2C_P	B4	U4	|	U9	B24	DP9_C2M_P
DP10_M2C_N	Y11	T1	|	T6	Z25	DP10_C2M_N
DP10_M2C_P	Y10	T2	|	T7	Z24	DP10_C2M_P
DP11_M2C_N	Z13	R3	|	R8	Y27	DP11_C2M_N
DP11_M2C_P	Z12	R4	|	R9	Y26	DP11_C2M_P
DP12_M2C_N	Y15	P1	|	P6	Z29	DP12_C2M_N
DP12_M2C_P	Y14	P2	|	P7	Z28	DP12_C2M_P
DP13_M2C_N	Z17	N3	|	N8	Y31	DP13_C2M_N
DP13_M2C_P	Z16	N4	|	N9	Y30	DP13_C2M_P
DP14_M2C_N	Y19	M1	|	M6	M19	DP14_C2M_N
DP14_M2C_P	Y18	M2	|	M7	M18	DP14_C2M_P
DP15_M2C_N	Y23	L3	|	L8	M23	DP15_C2M_N
DP15_M2C_P	Y22	L4	|	L9	M22	DP15_C2M_P
DP16_M2C_N	Z33	K1	|	K6	M27	DP16_C2M_N
DP16_M2C_P	Z32	K2	|	K7	M26	DP16_C2M_P

Table 48 : MGT Pins (continued on next page)

Signal	FMC (J1)	ACAP		ACAP	FMC (J1)	Signal
DP17_M2C_N	Y35	J3	|	K10	M31	DP17_C2M_N
DP17_M2C_P	Y34	J4	|	K11	M30	DP17_C2M_P
DP18_M2C_N	Z37	H1	|	J8	M35	DP18_C2M_N
DP18_M2C_P	Z36	H2	|	J9	M34	DP18_C2M_P
DP19_M2C_N	Y39	H5	|	H10	M39	DP19_C2M_N
DP19_M2C_P	Y38	H6	|	H11	M38	DP19_C2M_P
DP20_M2C_N	M15	G3	|	G8	Z9	DP20_C2M_N
DP20_M2C_P	M14	G4	|	G9	Z8	DP20_C2M_P
DP21_M2C_N	M11	F1	|	F10	Y7	DP21_C2M_N
DP21_M2C_P	M10	F2	|	F11	Y6	DP21_C2M_P
DP22_M2C_N	M7	F5	|	E8	Z5	DP22_C2M_N
DP22_M2C_P	M6	F6	|	E9	Z4	DP22_C2M_P
DP23_M2C_N	M3	E3	|	D10	Y3	DP23_C2M_N
DP23_M2C_P	M2	E4	|	D11	Y2	DP23_C2M_P

Table 48 : MGT Pins

Appendix F: MIO Map

Pin Number	Pin Name	Signal Name	Comment
F34	PMC_MIO0_500	QSPI0_CLK	Dual-Parallel Quad SPI
G34	PMC_MIO1_500	QSPI0_IO[1]	Dual-Parallel Quad SPI
H33	PMC_MIO2_500	QSPI0_IO[2]	Dual-Parallel Quad SPI
F33	PMC_MIO3_500	QSPI0_IO[3]	Dual-Parallel Quad SPI
E33	PMC_MIO4_500	QSPI0_IO[0]	Dual-Parallel Quad SPI
F32	PMC_MIO5_500	QSPI0_CS_b	Dual-Parallel Quad SPI
G32	PMC_MIO6_500	PMC_MIO_500_6	GPIO to Config Socket
H32	PMC_MIO7_500	QSPI1_CS_b	Dual-Parallel Quad SPI
K32	PMC_MIO8_500	QSPI1_IO[0]	Dual-Parallel Quad SPI
L32	PMC_MIO9_500	QSPI1_IO[1]	Dual-Parallel Quad SPI
M32	PMC_MIO10_500	QSPI1_IO[2]	Dual-Parallel Quad SPI
N32	PMC_MIO11_500	QSPI1_IO[3]	Dual-Parallel Quad SPI
N31	PMC_MIO12_500	QSPI1_CLK	Dual-Parallel Quad SPI
M31	PMC_MIO13_500	PMC_GPIO13	GPIO to VPX RTM
K31	PMC_MIO14_500	SMAP_D00	SMAP Interface
J31	PMC_MIO15_500	SMAP_D01	SMAP Interface
H31	PMC_MIO16_500	SMAP_D02	SMAP Interface
G31	PMC_MIO17_500	SMAP_D03	SMAP Interface
F30	PMC_MIO18_500	SMAP_CLK	SMAP Interface
G30	PMC_MIO19_500	SMAP_CS_B	SMAP Interface
J30	PMC_MIO20_500	SMAP_RDWR_B	SMAP Interface
K30	PMC_MIO21_500	SMAP_BUSY	SMAP Interface
L30	PMC_MIO22_500	SMAP_D04	SMAP Interface
M30	PMC_MIO23_500	SMAP_D05	SMAP Interface
M29	PMC_MIO24_500	SMAP_D06	SMAP Interface
L29	PMC_MIO25_500	SMAP_D07	SMAP Interface
B21	PMC_MIO26_501	PMC_MIO_500_26 / SD0_CLK	SMAP Interface / SDCARD
C21	PMC_MIO27_501	PMC_MIO_500_27	SMAP Interface
D21	PMC_MIO28_501	SMAP_D08	SMAP Interface
E21	PMC_MIO29_501	SMAP_D09 / SD0_CMD	SMAP Interface / SDCARD
F20	PMC_MIO30_501	SMAP_D10 / SD0_DATA0	SMAP Interface / SDCARD

Table 49 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
E20	PMC_MIO31_501	SMAP_D11 / SD0_DATA1	SMAP Interface / SDCARD
D20	PMC_MIO32_501	SMAP_D12 / SD0_DATA2	SMAP Interface / SDCARD
B20	PMC_MIO33_501	SMAP_D13 / SD0_DATA3	SMAP Interface / SDCARD
A20	PMC_MIO34_501	SMAP_D14	SMAP Interface
A19	PMC_MIO35_501	SMAP_D15	SMAP Interface
B19	PMC_MIO36_501	MIO36	GPIO to VPX (output)
C19	PMC_MIO37_501	MIO37	GPIO to VPX (output)
D19	PMC_MIO38_501	MIO38	GPIO to VPX (output)
F19	PMC_MIO39_501	MIO39	GPIO to VPX (output)
G19	PMC_MIO40_501	MIO40	GPIO to VPX (input)
F18	PMC_MIO41_501	MIO41	GPIO to VPX (input)
E18	PMC_MIO42_501	MIO42	GPIO to VPX (input)
D18	PMC_MIO43_501	MIO43	GPIO to VPX (input)
C18	PMC_MIO44_501	VOR_GPIO0	GPIO to Sysmon uC
A18	PMC_MIO45_501	VOR_GPIO1	GPIO to Sysmon uC
A17	PMC_MIO46_501	VOR_GPIO2	GPIO to Sysmon uC
B17	PMC_MIO47_501	VOR_GPIO3	GPIO to Sysmon uC
C17	PMC_MIO48_501	VOR_GPIO4	GPIO to Sysmon uC
E17	PMC_MIO49_501	VOR_GPIO5	GPIO to Sysmon uC
F17	PMC_MIO50_501	GEM0_MDIO_CLK	GEM0 Ethernet
G17	PMC_MIO51_501	GEM0_MDIO_DATA	GEM0 Ethernet
A39	LPD_MIO0_502	GEM0_TX_CLK	GEM0 Ethernet
B39	LPD_MIO1_502	GEM0_TX_DATA[0]	GEM0 Ethernet
C39	LPD_MIO2_502	GEM0_TX_DATA[1]	GEM0 Ethernet
C38	LPD_MIO3_502	GEM0_TX_DATA[2]	GEM0 Ethernet
A38	LPD_MIO4_502	GEM0_TX_DATA[3]	GEM0 Ethernet
A37	LPD_MIO5_502	GEM0_TX_CTRL	GEM0 Ethernet
B37	LPD_MIO6_502	GEM0_RX_CLK	GEM0 Ethernet
C37	LPD_MIO7_502	GEM0_RX_DATA[0]	GEM0 Ethernet
E37	LPD_MIO8_502	GEM0_RX_DATA[1]	GEM0 Ethernet
F37	LPD_MIO9_502	GEM0_RX_DATA[2]	GEM0 Ethernet
E36	LPD_MIO10_502	GEM0_RX_DATA[3]	GEM0 Ethernet
D36	LPD_MIO11_502	GEM0_RX_CTRL	GEM0 Ethernet
C36	LPD_MIO12_502	NC	Not Used

Table 49 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
B36	LPD_MIO13_502	SYSMON_I2C_SCL	Sysmon I2C bus
A35	LPD_MIO14_502	SYSMON_I2C_SDA	Sysmon I2C bus
B35	LPD_MIO15_502	SYSMON_I2C_ALERT	Sysmon I2C bus
D35	LPD_MIO16_502	UART0_RXD	UART0
E35	LPD_MIO17_502	UART0_RXD	UART0
F35	LPD_MIO18_502	PCIE_RST_MIO	Reset Input
G35	LPD_MIO19_502	PCIE_RST_MIO	Reset Input
D34	LPD_MIO20_502	MSP_MON_RX	Sysmon UART
C34	LPD_MIO21_502	MSP_MON_TX	Sysmon UART
B34	LPD_MIO22_502	I2C0_SCL	I2C to Config socket
A34	LPD_MIO23_502	I2C0_SDA	I2C to Config socket
C33	LPD_MIO24_502	CAN1_TX	CAN Interface 1
D33	LPD_MIO25_502	CAN1_RX	CAN Interface 1

Table 49 : MIO Map

Appendix G: DDR4 Pinout Table

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
AE38	DDR4_0_A<0>	700	0
AD41	DDR4_0_A<1>	700	0
AF38	DDR4_0_A<10>	700	0
AD42	DDR4_0_A<11>	700	0
AF46	DDR4_0_A<12>	700	0
AF43	DDR4_0_A<13>	700	0
AJ40	DDR4_0_A<14>	700	0
AH41	DDR4_0_A<15>	700	0
AE40	DDR4_0_A<2>	700	0
AG37	DDR4_0_A<3>	700	0
AF39	DDR4_0_A<4>	700	0
AF42	DDR4_0_A<5>	700	0
AE42	DDR4_0_A<6>	700	0
AG44	DDR4_0_A<7>	700	0
AD43	DDR4_0_A<8>	700	0
AC37	DDR4_0_A<9>	700	0
AF37	DDR4_0_ACT_N	700	0
AL42	DDR4_0_ALERT_N	701	0
AH38	DDR4_0_BA0	700	0
AF40	DDR4_0_BA1	700	0
AG39	DDR4_0_BG0	700	0
AG43	DDR4_0_BG1	700	0
AD38	DDR4_0_CKE	700	0
AF41	DDR4_0_CLK_C	700	0
AG41	DDR4_0_CLK_T	700	0
AH40	DDR4_0_CS_N	700	0
AN42	DDR4_0_DEBUG	701	0
AP40	DDR4_0_DM<0>	701	0
AK40	DDR4_0_DM<1>	701	0
AF47	DDR4_0_DM<2>	700	0
AH43	DDR4_0_DM<3>	700	0
AN46	DDR4_0_DM<4>	701	0
AT47	DDR4_0_DM<5>	701	0

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
BB46	DDR4_0_DM<6>	702	0
AY45	DDR4_0_DM<7>	702	0
AY42	DDR4_0_DM<8>	702	0
AN40	DDR4_0_DQ<0>	701	0
AR39	DDR4_0_DQ<1>	701	0
AM41	DDR4_0_DQ<10>	701	0
AK38	DDR4_0_DQ<11>	701	0
AM39	DDR4_0_DQ<12>	701	0
AL37	DDR4_0_DQ<13>	701	0
AK37	DDR4_0_DQ<14>	701	0
AM38	DDR4_0_DQ<15>	701	0
AJ47	DDR4_0_DQ<16>	700	0
AH47	DDR4_0_DQ<17>	700	0
AE46	DDR4_0_DQ<18>	700	0
AK46	DDR4_0_DQ<19>	700	0
AP39	DDR4_0_DQ<2>	701	0
AD47	DDR4_0_DQ<20>	700	0
AE47	DDR4_0_DQ<21>	700	0
AK47	DDR4_0_DQ<22>	700	0
AD45	DDR4_0_DQ<23>	700	0
AE44	DDR4_0_DQ<24>	700	0
AJ45	DDR4_0_DQ<25>	700	0
AF44	DDR4_0_DQ<26>	700	0
AJ44	DDR4_0_DQ<27>	700	0
AD44	DDR4_0_DQ<28>	700	0
AK45	DDR4_0_DQ<29>	700	0
AT39	DDR4_0_DQ<3>	701	0
AK44	DDR4_0_DQ<30>	700	0
AE45	DDR4_0_DQ<31>	700	0
AL46	DDR4_0_DQ<32>	701	0
AM46	DDR4_0_DQ<33>	701	0
AM45	DDR4_0_DQ<34>	701	0
AN47	DDR4_0_DQ<35>	701	0
AM44	DDR4_0_DQ<36>	701	0
AL47	DDR4_0_DQ<37>	701	0
AL44	DDR4_0_DQ<38>	701	0

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
AL43	DDR4_0_DQ<39>	701	0
AM37	DDR4_0_DQ<4>	701	0
AR44	DDR4_0_DQ<40>	701	0
AR45	DDR4_0_DQ<41>	701	0
AP43	DDR4_0_DQ<42>	701	0
AP44	DDR4_0_DQ<43>	701	0
AU44	DDR4_0_DQ<44>	701	0
AU45	DDR4_0_DQ<45>	701	0
AT44	DDR4_0_DQ<46>	701	0
AU46	DDR4_0_DQ<47>	701	0
BC46	DDR4_0_DQ<48>	702	0
AV46	DDR4_0_DQ<49>	702	0
AT41	DDR4_0_DQ<5>	701	0
AW47	DDR4_0_DQ<50>	702	0
BC47	DDR4_0_DQ<51>	702	0
AV47	DDR4_0_DQ<52>	702	0
AY46	DDR4_0_DQ<53>	702	0
BE46	DDR4_0_DQ<54>	702	0
BD47	DDR4_0_DQ<55>	702	0
AW45	DDR4_0_DQ<56>	702	0
BD45	DDR4_0_DQ<57>	702	0
AV45	DDR4_0_DQ<58>	702	0
BD44	DDR4_0_DQ<59>	702	0
AT40	DDR4_0_DQ<6>	701	0
AW44	DDR4_0_DQ<60>	702	0
BC45	DDR4_0_DQ<61>	702	0
BE45	DDR4_0_DQ<62>	702	0
AY44	DDR4_0_DQ<63>	702	0
BE42	DDR4_0_DQ<64>	702	0
BD42	DDR4_0_DQ<65>	702	0
BC43	DDR4_0_DQ<66>	702	0
AV43	DDR4_0_DQ<67>	702	0
AW42	DDR4_0_DQ<68>	702	0
AV42	DDR4_0_DQ<69>	702	0
AN38	DDR4_0_DQ<7>	701	0
BC42	DDR4_0_DQ<70>	702	0

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
AW43	DDR4_0_DQ<71>	702	0
AL41	DDR4_0_DQ<8>	701	0
AM40	DDR4_0_DQ<9>	701	0
AR41	DDR4_0_DQS0_C	701	0
AR42	DDR4_0_DQS0_T	701	0
AK39	DDR4_0_DQS1_C	701	0
AL39	DDR4_0_DQS1_T	701	0
AG46	DDR4_0_DQS2_C	700	0
AH46	DDR4_0_DQS2_T	700	0
AG45	DDR4_0_DQS3_C	700	0
AH45	DDR4_0_DQS3_T	700	0
AN45	DDR4_0_DQS4_C	701	0
AP45	DDR4_0_DQS4_T	701	0
AT46	DDR4_0_DQS5_C	701	0
AR46	DDR4_0_DQS5_T	701	0
BA46	DDR4_0_DQS6_C	702	0
AY47	DDR4_0_DQS6_T	702	0
BB45	DDR4_0_DQS7_C	702	0
BB44	DDR4_0_DQS7_T	702	0
BA42	DDR4_0_DQS8_C	702	0
BB43	DDR4_0_DQS8_T	702	0
AD39	DDR4_0_ODT	700	0
AD40	DDR4_0_PARITY	700	0
AD37	DDR4_0_RAS_N	700	0
AK42	DDR4_0_RESET_N	701	0
AN43	MEM_CLK_0_N	701	0
AM43	MEM_CLK_0_P	701	0
BE27	DDR4_1_A<0>	705	1
BC26	DDR4_1_A<1>	705	1
BG28	DDR4_1_A<10>	705	1
AV29	DDR4_1_A<11>	705	1
AP27	DDR4_1_A<12>	705	1
AY27	DDR4_1_A<13>	705	1
BB28	DDR4_1_A<14>	705	1
BD29	DDR4_1_A<15>	705	1
BB26	DDR4_1_A<2>	705	1

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
BG30	DDR4_1_A<3>	705	1
BD27	DDR4_1_A<4>	705	1
AW25	DDR4_1_A<5>	705	1
AW27	DDR4_1_A<6>	705	1
AU27	DDR4_1_A<7>	705	1
AW28	DDR4_1_A<8>	705	1
BF26	DDR4_1_A<9>	705	1
BF28	DDR4_1_ACT_N	705	1
BA32	DDR4_1_ALERT_N	704	1
BG29	DDR4_1_BA0	705	1
BC27	DDR4_1_BA1	705	1
BF29	DDR4_1_BG0	705	1
AY26	DDR4_1_BG1	705	1
BE26	DDR4_1_CKE	705	1
BD28	DDR4_1_CLK_C	705	1
BC28	DDR4_1_CLK_T	705	1
BD30	DDR4_1_CS_N	705	1
AW31	DDR4_1_DEBUG	704	1
AV26	DDR4_1_DM<0>	705	1
AR26	DDR4_1_DM<1>	705	1
AR33	DDR4_1_DM<2>	704	1
AR30	DDR4_1_DM<3>	704	1
BE31	DDR4_1_DM<4>	704	1
BD33	DDR4_1_DM<5>	704	1
BD37	DDR4_1_DM<6>	703	1
AW36	DDR4_1_DM<7>	703	1
AT38	DDR4_1_DM<8>	703	1
AU29	DDR4_1_DQ<0>	705	1
AT28	DDR4_1_DQ<1>	705	1
AP25	DDR4_1_DQ<10>	705	1
AM27	DDR4_1_DQ<11>	705	1
AM26	DDR4_1_DQ<12>	705	1
AM29	DDR4_1_DQ<13>	705	1
AN25	DDR4_1_DQ<14>	705	1
AN28	DDR4_1_DQ<15>	705	1
AP34	DDR4_1_DQ<16>	704	1

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
AR32	DDR4_1_DQ<17>	704	1
AU33	DDR4_1_DQ<18>	704	1
AP33	DDR4_1_DQ<19>	704	1
AT25	DDR4_1_DQ<2>	705	1
AV34	DDR4_1_DQ<20>	704	1
AV33	DDR4_1_DQ<21>	704	1
AN34	DDR4_1_DQ<22>	704	1
AW33	DDR4_1_DQ<23>	704	1
AU31	DDR4_1_DQ<24>	704	1
AN31	DDR4_1_DQ<25>	704	1
AT31	DDR4_1_DQ<26>	704	1
AM30	DDR4_1_DQ<27>	704	1
AV31	DDR4_1_DQ<28>	704	1
AM32	DDR4_1_DQ<29>	704	1
AT26	DDR4_1_DQ<3>	705	1
AV30	DDR4_1_DQ<30>	704	1
AM33	DDR4_1_DQ<31>	704	1
BF31	DDR4_1_DQ<32>	704	1
BB30	DDR4_1_DQ<33>	704	1
BF32	DDR4_1_DQ<34>	704	1
BC32	DDR4_1_DQ<35>	704	1
BB31	DDR4_1_DQ<36>	704	1
BB33	DDR4_1_DQ<37>	704	1
BE32	DDR4_1_DQ<38>	704	1
BG31	DDR4_1_DQ<39>	704	1
AR29	DDR4_1_DQ<4>	705	1
BF34	DDR4_1_DQ<40>	704	1
BG35	DDR4_1_DQ<41>	704	1
BG34	DDR4_1_DQ<42>	704	1
BE35	DDR4_1_DQ<43>	704	1
BC33	DDR4_1_DQ<44>	704	1
BD34	DDR4_1_DQ<45>	704	1
BB34	DDR4_1_DQ<46>	704	1
BD35	DDR4_1_DQ<47>	704	1
BD40	DDR4_1_DQ<48>	703	1
BC40	DDR4_1_DQ<49>	703	1

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
AV25	DDR4_1_DQ<5>	705	1
BB36	DDR4_1_DQ<50>	703	1
BC38	DDR4_1_DQ<51>	703	1
BB35	DDR4_1_DQ<52>	703	1
BB38	DDR4_1_DQ<53>	703	1
BC35	DDR4_1_DQ<54>	703	1
BC36	DDR4_1_DQ<55>	703	1
AY39	DDR4_1_DQ<56>	703	1
AW35	DDR4_1_DQ<57>	703	1
AW39	DDR4_1_DQ<58>	703	1
AV35	DDR4_1_DQ<59>	703	1
AT29	DDR4_1_DQ<6>	705	1
AU37	DDR4_1_DQ<60>	703	1
AU35	DDR4_1_DQ<61>	703	1
AY35	DDR4_1_DQ<62>	703	1
AU36	DDR4_1_DQ<63>	703	1
AR37	DDR4_1_DQ<64>	703	1
AT35	DDR4_1_DQ<65>	703	1
AR35	DDR4_1_DQ<66>	703	1
AM35	DDR4_1_DQ<67>	703	1
AP38	DDR4_1_DQ<68>	703	1
AM36	DDR4_1_DQ<69>	703	1
AU25	DDR4_1_DQ<7>	705	1
AP36	DDR4_1_DQ<70>	703	1
AN35	DDR4_1_DQ<71>	703	1
AN26	DDR4_1_DQ<8>	705	1
AN29	DDR4_1_DQ<9>	705	1
AV27	DDR4_1_DQS0_C	705	1
AU28	DDR4_1_DQS0_T	705	1
AR27	DDR4_1_DQS1_C	705	1
AP28	DDR4_1_DQS1_T	705	1
AT32	DDR4_1_DQS2_C	704	1
AU32	DDR4_1_DQS2_T	704	1
AP31	DDR4_1_DQS3_C	704	1
AN32	DDR4_1_DQS3_T	704	1
BC30	DDR4_1_DQS4_C	704	1

Table 50 : DDR4 Pinout Table (continued on next page)

Pin Number	Signal Name	ACAP Bank	DDR4 Bank
BC31	DDR4_1_DQS4_T	704	1
BG33	DDR4_1_DQS5_C	704	1
BF33	DDR4_1_DQS5_T	704	1
BD38	DDR4_1_DQS6_C	703	1
BD39	DDR4_1_DQS6_T	703	1
AW37	DDR4_1_DQS7_C	703	1
AV38	DDR4_1_DQS7_T	703	1
AP37	DDR4_1_DQS8_C	703	1
AR36	DDR4_1_DQS8_T	703	1
BF27	DDR4_1_ODT	705	1
BA27	DDR4_1_PARITY	705	1
BG26	DDR4_1_RAS_N	705	1
BA33	DDR4_1_RESET_N	704	1
BA31	MEM_CLK_1_N	704	1
AY31	MEM_CLK_1_P	704	1

Table 50 : DDR4 Pinout Table

Appendix H: Vorago Pin Assignments

Appendix H.1: Ethernet Pins (P3 Wafers 11-13)

Signal	VPX P3		VPX P3	Signal
ETHB_OUT_0_N	B11	|	C12	ETHB_OUT_2_N
ETHB_OUT_0_P	A11	|	B12	ETHB_OUT_2_P
ETHB_OUT_1_N	E11	|	F12	ETHB_OUT_3_N
ETHB_OUT_1_P	D11	|	E12	ETHB_OUT_3_P
ETHB_LED0	A13	|	B13	ETHB_LED1

Table 51 : Ethernet (P3 Wafers 11-13)

Appendix H.2: Serial Interfaces (P3 Wafers 10,14)

Signal	VPX P3	Notes
VOR_UART_RX	C10	UART RX
VOR_UART_TX	B10	UART TX
CANVH	B14	CAN BUS H
CANVL	C14	CAN BUS L
VOR_SCL2	E14	I2C CLK
VOR_SDA2	F14	I2C DAT

Table 52 : Serial Interfaces (P3 Wafers 10,14)

Appendix H.3: GPIO (P3 Wafers 15-16)

Signal	VPX P3	uC pin		uC pin	VPX P3	Signal
GPIOV<0>	A15	75	|	76	B15	GPIOV<1>
GPIOV<2>	D15	77	|	78	E15	GPIOV<3>
GPIOV<4>	B16	79	|	83	C16	GPIOV<5>
GPIOV<6>	E16	84	|	85	F16	GPIOV<7>
OE_L	-	39	|	38	-	DIR

Table 53 : GPIO (P3 Wafers 15-16)

Revision History

Date	Revision	Nature of Change
01 Apr 2024	0.1	Initial Draft
15 Nov 2024	0.2	After first review
03 Feb 2025	1.0	First release

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